Notice of Allowability	Application No.	Applicant(s)
	10/042,031	BUDELL ET AL.
	Examiner	Art Unit
	Jeremy C. Norris	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *telephonic Interview held 24 August 2005*.

2. ☒ The allowed claim(s) is/are *3, 5, 6, 13, 15, 16, 20, 21, 22, 24, and 27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jack Friedman on 24 August 2005.

The application has been amended as follows: in the claims,

CANCEL claims 1, 2, 4, 7-12, 14, 17-19, 23, 25, 26 and 28.

REPLACE claim 21 with the following:

"21. (Amended) An electrical structure, comprising:

a dielectric substrate having a metal signal line therein; and

a first metal voltage plane laminated to a first surface of the dielectric substrate, wherein the first metal voltage plane includes an opening, wherein an image of a first portion of the metal signal line projects across the opening in the first metal voltage plane, and wherein a first electrically conductive strip across the opening in the first metal voltage plane includes the image of the first portion and wherein the opening in the first metal voltage plane has an outer boundary whose shape is circular or elliptical, [The electrical structure of claim 1,] wherein the first metal voltage plane comprises a first metal, wherein the first electrically conductive strip comprises a second metal, and wherein the first metal differs from the second metal."

REPLACE claim 22 with the following"

"22. (Amended) A method for forming an electrical structure, comprising:

providing a dielectric substrate having a metal signal line therein;

laminating a first metal voltage plane to a first surface of the dielectric substrate; and forming an opening in the first metal voltage plane such that a first electrically conductive strip across the opening includes an image of a first portion of the metal signal line, wherein the image of the first portion of the metal signal line projects across the opening in the first metal voltage plane and wherein the opening in the first metal voltage plane has an outer boundary whose shape is circular or elliptical, [The method of claim 11,] wherein the first metal voltage plane comprises a first metal, wherein the first electrically conductive strip comprises a second metal, and wherein the first metal differs from the second metal."

REPLACE claim 24 with the following:

"24. (Amended). A method for forming an electrical structure, comprising the steps of:

providing a dielectric substrate having a metal signal line therein;

laminating a first metal voltage plane to a first surface of the dielectric substrate; and forming an opening in the first metal voltage plane such that a first electrically conductive strip across the opening includes an image of a first

portion of the metal signal line, wherein the image of the first portion of the metal signal line projects across the opening in the first metal voltage plane, and wherein step of laminating the first metal voltage plane to the first surface of the dielectric substrate is performed before the step of forming the opening in the first metal voltage plane, [The method of claim 23,] wherein the first metal voltage plane comprises a first metal, wherein the first electrically conductive strip comprises a second metal and wherein the first metal differs from the second metal."

REPLACE claim 27 with the following:

27 (Amended). A method for forming an electrical structure, comprising the steps of:

providing a dielectric substrate having a metal signal line therein;

laminating a first metal voltage plane to a first surface of the dielectric substrate; and forming an opening in the first metal voltage plane such that a first electrically conductive strip across the opening includes an image of a first portion of the metal signal line, wherein the image of the first portion of the metal signal line projects across the opening in the first metal voltage plane, and wherein step of laminating the first metal voltage plane to the first surface of the dielectric substrate is performed after the step of forming the opening in the first metal voltage plane, [The method of claim 26,] wherein the first metal voltage plane comprises a first metal, wherein the first electrically conductive strip

comprises a second metal and wherein the first metal differs from the second metal."

Allowable Subject Matter

Claims 3, 5, 6, 13, 15, 16, 20, 21, 22, 24, and 27 are allowed.

The following is an examiner's statement of reasons for allowance: **Claims 3 and 13** state the limitation "wherein the first electrically conductive strip is not integral with the first metal voltage plane". The word integral has been examined in light of its plain meaning, i.e. "formed as a unit with another part". Therefore, "not integral" is examined as distinct and separate parts. In light of this definition, this limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. **Claims 5 and 15** state the limitation "wherein the first electrically conductive strip is nonlinear across the opening in the first metal voltage plane". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. **Claims 6 and 16** state the limitation "wherein the opening in the first metal voltage plane has a vent area of no less than about 0.1 square millimeters". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. **Claim 20** states the limitation "determining at least one problematic opening of the opening, wherein the at least one problematic opening is above or below a corresponding metal signal lines within the dielectric laminate such that an image of a portion of the corresponding metal signal lines projects across the at least one problematic opening". Applicant has supplied the specific definition "A problematic opening is defined herein

as an opening that is above or below a corresponding metal signal line within the dielectric laminate such that an image of a portion of the corresponding metal signal line projects across the problematic opening, such that the problematic opening results in unacceptably degraded electrical performance. In light of this definition, this limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. **Claims 21, 22, 24, and 27** state the limitation "wherein the first metal voltage plane comprises a first metal, wherein the first electrically conductive strip comprises a second metal, and wherein the first metal differs from the second metal". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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